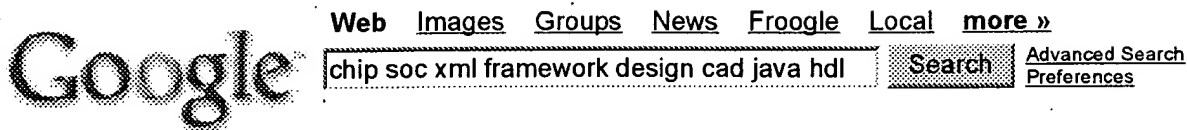


Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	67	xml and (cad) and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 19:22
L2	0	L1 and ("104.1").ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 19:23
L3	8	L1 and ("707/104.1").ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 19:23
S1	1	(collaborat\$3 near design) and (IP near design)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:24
S2	4	(collaborat\$3 near design) and (soc)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:17
S3	9	(collaborat\$3 near design) and (design near web)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:25
S4	5	S3 and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:25
S5	16	(collaborat\$3 near design) and (design near web\$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:26

S6	5	S5 and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:26
S7	9	(collaborat\$3 near web) and (design near web\$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:26
S8	5	S7 and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:27
S9	13	(web\$5 near design) and soc and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:30
S10	2	S9 and xml	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:27
S11	2	(web\$5 near design) and (system near chip) and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:32
S12	0	(framework near design) and xml and (system near chip) and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:33
S13	5	xml and (system near chip) and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:36

S14	67	xml and (cad) and @ad<"20010423"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:36
S15	13	S14 and (system same (chip or card))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:41
S16	10	S14 and (system same (chip or card)) and web	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 16:37
S17	5	S14 and (design same (chip or card))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/25 19:22

**Web**Results 1 - 10 of about 256 for **chip soc xml framework design cad java hdl**. (0.28 seconds)University Booth Table

... **Java-HDL** technique allow us to explore rapidly other **designs** spaces. ...
 Complex system-on-a-chip **design** requires more and more IP modules from 3rd ...
www.sigda.org/programs/UniversityBooth/Ubooth2001/info.html - 75k - [Cached](#) - [Similar pages](#)

OpenCollector Database

... for easy integration of Verilog IP cores for System-on-Chip (**SoC**) **designs**.
 ... JHDL is a set of FPGA **CAD** tools which allows the user to **design** the ...
opencollector.org/summary.php - 96k - Jul 23, 2005 - [Cached](#) - [Similar pages](#)

OpenCollector Database

... is an application which takes an **XML** definition of a ... Balsa: Balsa is both a **framework**
 for synthesising ... property (IP) cores for System-on-Chip (**SoC**) **designs**. ...
opencollector.org/summary.php3/images/get_details.php3 - 101k - Supplemental Result -
[Cached](#) - [Similar pages](#)

Participants

A memory failure analysis **framework** will be presented to identify **design** flaws
 ... system-on-chip (**SOC**) **design** to distributed heterogeneous system **design**. ...
users.ece.gatech.edu/lmsk/ubooth/detail03.html - 91k - [Cached](#) - [Similar pages](#)

EDACafe Weekly Magazine - February 10, 2003

The Debussy system is used for VLSI (ASIC and **SOC**) **design** understanding and ...
 The **chip** includes an 8052 processor, a USB interface, two built-in smart ...
www01.edatoolscafe.com/magazine/index.php?run_date=10-Feb-2003&newsletter=1 - 47k -
[Cached](#) - [Similar pages](#)

[PDF] DESIGN AUTOMATION SOLUTIONS FOR EUROPE

File Format: PDF/Adobe Acrobat - [View as HTML](#)
 What are the human implications in **SoC Design** ? On a single **chip**, **SoC** will put the
 ... The **design framework** for SoCs will have to manage a growth of ...
public.itrs.net/Files/2003ITRS/LinkedFiles/Design/MEDEA2002EDARoadmap.pdf - [Similar pages](#)

Things

The low-power **design** employed an ARM1136JF-S test **chip**, ARM Artisan standard ...
 System Generator for DSP is the **framework** for developing and debugging high ...
www.aycinena.com/index2/index3/archive/things%2023%20march%202005.html - 45k - [Cached](#) - [Similar pages](#)

SurfWax: News, Reviews and Articles On Design Tools

Researcher calls for 'software-centric' **SoC design** Jul 13, 2005 ... 0 physical
design tool, featuring on-chip-variation modeling, is the No. ...
news.surfwax.com/engineering/files/Design_Tools.html - 52k - [Cached](#) - [Similar pages](#)

[PPT] Design Productivity Crisis

File Format: Microsoft Powerpoint 97 - [View as HTML](#)
 Result: Must solve today's **design** problems with yesterday's **CAD** technology ...
 complete prototype of METRICS system with Oracle8i, **Java** Servlet, **XML** parser, ...
visicad.ucsd.edu/~abk/TALKS/japan-da-abk-final.ppt - [Similar pages](#)

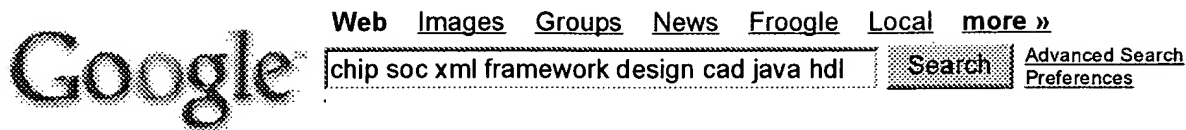
Digitized by Google

Google Desktop Search 9:30 AM

chip soc xml framework design cad j

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

<http://www.google.com/search?hl=en&lr=&q=chip+soc+xml+framework+design+cad+jav...> 7/25/2005

**Web**Results 1 - 10 of about 256 for **chip soc xml framework design cad java hdl**. (0.28 seconds)University Booth Table

... **Java-HDL** technique allow us to explore rapidly other **designs** spaces. ...
 Complex system-on-a-**chip design** requires more and more IP modules from 3rd ...
www.sigda.org/programs/UniversityBooth/Ubooth2001/info.html - 75k - [Cached](#) - [Similar pages](#)

OpenCollector Database

... for easy integration of Verilog IP cores for System-on-Chip (**SoC**) **designs**.
 ... JHDL is a set of FPGA **CAD** tools which allows the user to **design** the ...
opencollector.org/summary.php - 96k - Jul 23, 2005 - [Cached](#) - [Similar pages](#)

OpenCollector Database

... is an application which takes an **XML** definition of a ... Balsa: Balsa is both a **framework** for synthesising ... property (IP) cores for System-on-Chip (**SoC**) **designs**. ...
opencollector.org/summary.php3/images/get_details.php3 - 101k - Supplemental Result -
[Cached](#) - [Similar pages](#)

Participants

A memory failure analysis **framework** will be presented to identify **design** flaws
 ... system-on-**chip (SOC)** **design** to distributed heterogeneous system **design**. ...
users.ece.gatech.edu/lmsk/ubooth/detail03.html - 91k - [Cached](#) - [Similar pages](#)

EDACafe Weekly Magazine - February 10, 2003

The Debussy system is used for VLSI (ASIC and **SoC**) **design** understanding and ...
 The **chip** includes an 8052 processor, a USB interface, two built-in smart ...
www01.edatoolscafe.com/magazine/index.php?run_date=10-Feb-2003&newsletter=1 - 47k -
[Cached](#) - [Similar pages](#)

[PDF] DESIGN AUTOMATION SOLUTIONS FOR EUROPE

File Format: PDF/Adobe Acrobat - [View as HTML](#)
 What are the human implications in **SoC Design** ? On a single **chip**, **SoC** will put the
 ... The **design framework** for SoCs will have to manage a growth of ...
public.itrs.net/Files/2003ITRS/LinkedFiles/Design/MEDEA2002EDARoadmap.pdf - [Similar pages](#)

Things

The low-power **design** employed an ARM1136JF-S test **chip**, ARM Artisan standard ...
 System Generator for DSP is the **framework** for developing and debugging high ...
www.aycinena.com/index2/index3/archive/things%2023%20march%202005.html - 45k - [Cached](#) - [Similar pages](#)

SurfWax: News, Reviews and Articles On Design Tools

Researcher calls for 'software-centric' **SoC design** Jul 13, 2005 ... 0 physical
design tool, featuring on-**chip**-variation modeling, is the No. ...
news.surfwax.com/engineering/files/Design_Tools.html - 52k - [Cached](#) - [Similar pages](#)

[PPT] Design Productivity Crisis

File Format: Microsoft Powerpoint 97 - [View as HTML](#)
 Result: Must solve today's **design** problems with yesterday's **CAD** technology ...
 complete prototype of METRICS system with Oracle8i, Java Servlet, **XML** parser, ...
vlsicad.ucsd.edu/~abk/TALKS/japan-da-abk-final.ppt - [Similar pages](#)

Digitized by Google

Google Desktop Search 9:30 AM

chip soc xml framework design cad j Search

<http://www.google.com/search?hl=en&lr=&q=chip+soc+xml+framework+design+cad+jav...> 7/25/2005